

# COM420/2PC

Dual Current-Loop Asynchronous Communications Adapter

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**COM420/2PC  
User's Manual**

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# COM420/2PC User's Manual

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## 1.1 Introduction

The COM420/2PC is a two channel, asynchronous, current loop communication board which occupies only one expansion slot within the users personal computer. Two channels are provided by two 8250 UART's (universal asynchronous receiver transmitter) which allows the user to communicate to two independent serial devices. The COM420/2PC supports data transfer rates up to 19200 baud.

The COM420/2PC supports all forms of active and passive current loop communication. Each serial port uses three switch banks which allow the user to configure that particular serial port. One switch bank controls transmission while the other two switch banks control reception.

The COM420/2PC is a 7.5 inch printed circuit board which is larger then a half size printed circuit board but smaller then a full size printed circuit board. Each serial port contains its own fourteen position address switch (one eight position switch plus a six position switch). This switch allows the user to install the COM420/2PC in an address range from 0000H to FFFFH within his or her personal computer. The COM420/2PC may therefore be implemented as COM1, COM2, COM3, COM4, etc. Interrupts 2-7 are also made available to the user via a twelve position male header. Any one of these interrupts may be selected by placing a jumper block on two of the appropriate pins. It is also possible for the COM420/2PC to share an interrupt with another device such as IOtech's COM232/4PC, COM422/4PC or COM485/4PC. All transmit and receive signals are made available via a DB-9 connector. The output handshake signal RTS is connected to the input handshake signal CTS while the output handshake signal DTR is connected to the input handshake signals DSR, CD, and RI.

The COM420/2PC offers the user a versatile and inexpensive alternative to interfacing his or her personal computer to any serial device requiring current loop communication. No longer will the user have to purchase both serial peripheral boards and converter boxes to accomplish the task of current loop communication.

In the following pages, a step by step approach is taken to guide the user in configuring and installing the COM420/2PC. If any problems arise, please feel free to contact the IOtech applications department at (216) 439-4091.

### NOTE

**The optional 16550 ACE has been installed within your IOtech COM420/2PC board.**

## 1.2 Specifications

### COM420/2PC PARTS LAYOUT

**Current Loop Transmitter:**

Active transmit total loop voltage: +12v(typ.)  
Space state transmitter voltage drop: .3v (typ.)  
Mark state transmitter voltage drop: 1.5v (typ.)  
Optical isolation voltage: 3000v (max)

**Current Loop Receiver:**

Active receive total loop voltage: +12v (typ.)  
Space state receiver voltage drop: 1.1v (typ.)  
Mark state receiver voltage drop: 2.5v (typ.)  
Optical isolation: 3000v (max)

**DC-DC Converter:**

Input voltage: 5v  
Output voltage: 12v  
Output current: 125mA

**Baudrate:** 19200 bits/sec (max.)

**Power Consumption:**

+5V : 266mA (typ.) 399mA (max.)  
-5V : not used  
+12V: 100mA (typ.) 125mA (max.)  
-12V: not used

**Board Dimensions:** 9.9125" x 4.2000"

## 1.3 Installing the COM420/2PC

Thank you for purchasing the COM420/2PC Dual Current Loop Serial Communication Board. The COM420/2PC offers both an easy and inexpensive approach to interfacing the personal computer with equipment requiring current loop communication.

The following section explains how to configure the COM420/2PC to meet your particular application needs and the steps necessary to properly configure the COM420/2PC prior to installation within the personal computer. The initial board setup can be broken down into three areas:

- Address Selection
- Jumper and Switch Settings
- Connector Cabling

## 1.3.1 Address Selection

### 1.3.1.1 Address Space Used By The COM420/2PC

Every device that is to be installed into a personal computer via one of its expansion slots must be assigned a unique address so the microprocessor or CPU (central processing unit) may communicate with that device. Since the COM420/2PC contains two devices, serial ports 1 and 2, two unique addresses must be assigned to each device. It is very important that two or more devices are not assigned the same address.

When the microprocessor requests information such as data or status from a device, it does so by sending out an address and the device which resides at that address responds. If two or more devices reside at the same address, they all "speak" to the microprocessor at the same time, and as many of you know when two or more people speak to you at the same time, you don't know what's going on! That's exactly what happens, the microprocessor does not know what's going on, so he responds to the user by "hanging up" his computer, returning erroneous information, etc.

Therefore, the first order of business is to assign each one of the two serial ports a unique address (this is defined as a BASE ADDRESS). The base address of serial port 1 is set by the fourteen position dip switch formed by dip switches SW1 and SW3, while the base address of serial port 2 is set by the fourteen position dip switch formed by dip switches SW2 and SW4. Each fourteen position dip switch allows its respective device to reside anywhere in the I/O port address space from 0000H - FFFFH on eight byte boundaries.

An eight byte boundary simply implies that each of the serial ports use eight consecutive addresses of the I/O address space. For example, if the base address of the first serial port is set to 3F8H then that serial port occupies addresses 3F8H-3FFH. The serial ports require eight addresses to access their eight internal registers (refer to Figure 1 for a complete list of the above mentioned serial ports internal registers).

Although the serial ports of the COM420/2PC may be assigned any base address from 0000H to FFFFH as dictated by SW1-SW4, the recommended allowable I/O spaces for the IBM PC/XT/AT are represented by Figure 2. The user may select any address outside these ranges but within 0000H to FFFFH provided no other device is installed at that address.

### 1.3.1.2 Base Address Assignment

The majority of plug in boards are defined as I/O mapped. An I/O mapped device utilizes the I/O read and write signals (-IOR and -IOW) of the microprocessor. A memory mapped device utilizes the memory read and write signals (-MEMR and -MEMW) of the microprocessor. The I/O mapped board uses only sixteen of the twenty address bits provided by the computer. The COM420/2PC uses all sixteen of these address bits. The dip switches SW1 (serial port #1) and SW2 (serial port #2) allow user-selection of the eight upper address bits, A8-A15.

Dip switches SW3 (serial port #1) and SW4 (serial port #2) allow user-selection of the five lower address bits, A3-A7. Address bits A0, A1, and A2 are not user selectable by SW1-SW4 since they are used to access the eight addresses occupied by the serial ports. Position 6 of dip switches SW3 and SW4 is used as a master enable/disable for serial ports 1 and 2 respectively. Placing position 6 in the 'ON' position enables its respective serial port and placing it in the 'OFF' position disables its respective serial port. The two examples that follow illustrate how the address bits are associated with the switch positions. Setting each switch position to ON or OFF sets the corresponding address bit to a 0 or 1 respectively. The binary value corresponding to the switch position is listed below the switch illustration. The binary value is then converted to its hexadecimal equivalent. This hexadecimal number is the base address.

DLAB	A2	A1	A0	Register Description
0	0	0	0	Receive buffer (read only) Transmitter holding register (write only)
0	0	0	1	Interrupt enable
x	0	1	0	Interrupt identification (read only) FIFO control* (write only)
x	0	1	1	Line control
x	1	0	0	MODEM control
x	1	0	1	Line status
x	1	1	0	MODEM status
x	1	1	1	Scratch
1	0	0	0	Divisor latch (LSB)
1	0	0	1	Divisor latch (MSB)

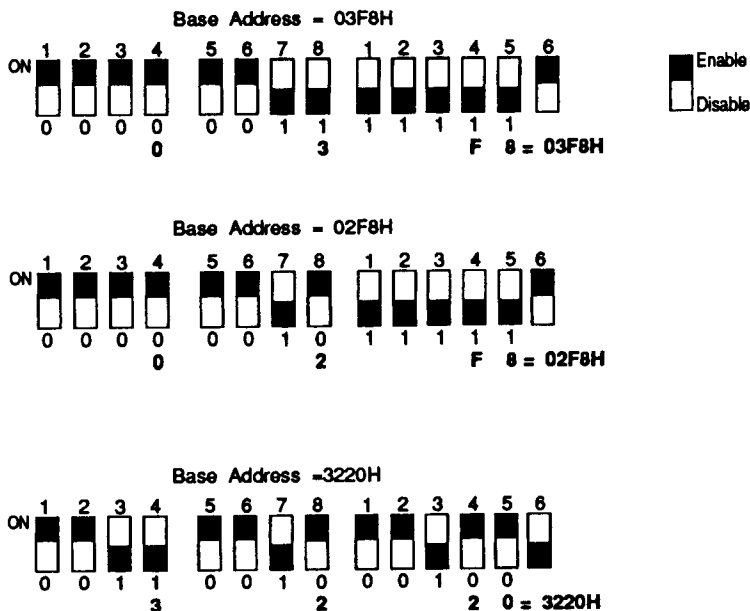
Figure 1: 8250/16450 Internal Register Map



Address Range	Device
000-01FH	DMA Controller Chip #1 8237A
020-03FH	Interrupt Controller Chip #1 8259A
040-05FH	Timer Chip 8254
060-06FH	Keyboard Chip 8042
070-07FH	Real Time Clock (Non-Maskable Interrupt)
080-09FH	DMA Page Register Chip 74LS612
0A0-0BFH	Interrupt Controller Chip #2 8259A
0C0-0DFH	DMA Controller Chip #2 8237A
0F0H	Clear Math Coprocessor Busy
0F1H	Reset Math Coprocessor
0F8-0FFH	Math Coprocessor
1F0-1F8H	Fixed Disk (Hard Disk)
200-207H	Gameport
278-27FH	Parallel Printer Port #2
2F8-2FFH	Serial Port #2
300-31FH	Prototype Board
360-36FH	Reserved
378-37FH	Parallel Printer Port #1
380-38FH	SDLC BISYNC Port #2
3A0-3AFH	BISYNC Port #1
3B0-3BFH	Monochrome Display & Parallel Printer Port #1
3C0-3CFH	Reserved
3D0-3DFH	Color Graphics Monitor Adapter
3F0-3F7H	Diskette Controller
3F8-3FFH	Serial Port #1

**Figure 2: Reserved I/O Address Map**

### 1.3.1.3 Base Address Assignment Examples



**Figure 3: Base Address Examples**

### 1.3.1.4 Factory Address Settings

IOtech assigns the following base addresses to each of the serial ports:

SERIAL PORT #1 :      COM1 @ 3F8H

SERIAL PORT #2 :      COM2 @ 2F8H

The COM420/2PC is shipped with the above base address assignments.

It is worth mentioning at this time the addresses IBM assigns to COM1-COM8.

COM1	@ 3F8H
COM2	@ 2F8H
COM3	@ NOT DECLARED
COM4	@ NOT DECLARED
COM5	@ NOT DECLARED
COM6	@ NOT DECLARED
COM7	@ NOT DECLARED
COM8	@ NOT DECLARED

DOS relates physical communication devices to logical names such as COM1, COM2, LPT1, LPT2, and LPT3. Three printer interfaces and two serial interfaces are supported by DOS. Upon bootup, DOS checks certain addresses for installed devices and assigns them a logical name. DOS checks for parallel port interfaces at the following addresses in the following order: 03BCH, 0378H, 0278H. DOS assigns the logical name LPT1 to the first parallel interface it finds installed, LPT2 to the second and LPT3 to the third. DOS checks for serial port interfaces at the following addresses in the following order : 3F8H, 2F8H. COM1 is assigned to the first serial port DOS recognizes and COM2 is assigned to the second.

## 1.4 Configurations

There are five jumper blocks and five dip switches which are used to select a particular feature of the COM420/2PC when more then one feature is available. The jumper blocks are designated J1-J5 while the dip switches are designated SW5-SW9.

### 1.4.1 J1-Clock Select

J1 is a six position jumper block which is used to divide the on board oscillator frequency by 1, 2, 5, or 10, depending upon J1's configuration, and then provide this divided clock to the serial port UART chips (refer to figure 4). The on board oscillator has a frequency of 18.432 MHz. When pins 2&5 are connected on J1, a divider of 1 is selected and the serial port UART chips receive a clock input of 18.432 MHz. When pins 4&5 and 2&3 are connected on J1, a divider of 2 is selected and the serial port UART chips receive a clock input of 9.216 MHz. When pins 4&5 and 1&2 are connected on J1, a divider of 5 is selected and the serial port UART chips receive a clock input of 3.6864 MHz. Finally, connection

of pins 4&5, 1&2, and 3&6 yields a divider of 10 and the serial port UART chips receive a clock input of 1.8432 MHz.

The COM420/2PC is shipped with pins 4&5, 1&2, and 3&6 connected on J1 which selects a divider of 10. The UART chips which are installed on the COM420/2PC may receive a maximum clock input of 3.1 MHz. Therefore, J1 should never be configured for a divider of 1, 2, or 5 unless the UART chips can handle the resulting clock input. Such specialized UART chips do exist in the market which account for the additional dividers provided by jumper block, J1.

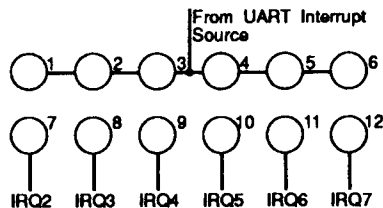
### 1.4.2 J2-Serial Port #1 Interrupt Select

J2 is a twelve position jumper block which selects the desired interrupt level, IRQ2-IRQ7, to be used by serial port #1 (refer to figure 5). The interrupt level selected may be shared with another device provided that device possesses interrupt sharing capabilities. The interrupt vectors for the IBM PC/XT/AT are as follows:

IRQ2:	28H-2BH
IRQ3:	2CH-2FH
IRQ4:	30H-33H
IRQ5:	34H-37H
IRQ6:	38H-3BH
IRQ7:	3CH-3FH

### 1.4.3 J3-Serial Port #2 Interrupt Select

J3 performs the same function as J2 except that it applies to serial port #2 (see the figure below).



**Figure 3: J3-Serial Port #2 Interrupt Select**

#### 1.4.4 J4 & J5-Isolated Power Supply Select

The COM420/2PC is equipped with two power supply options for generating the desired current level (20, 30, or 60 mA) within the communication loop (refer to figure 5). The computers power supply may be selected to generate the loop current by connecting pins 2&3 of J4 and pins 2&3 of J5. For more demanding industrial applications, an isolated DC-DC converter may be chosen to generate the loop current by connection pins 1&2 of J4 and pins 1&2 of J5.

#### 1.4.5 SW5(SW6)-Port #1(#2) Transmission Select

Serial port #1(#2) uses the eight position dip switch, SW5(SW6), to select either active or passive transmission (active transmission provides the current in the loop whereas passive transmission does not) and the value of current (20, 30, or 60 mA) when the active option is selected. Passive transmission is controlled by switch positions 1&2 and active transmission is controlled by switch positions 3&4. Switch positions 5-7 configure the value of current within the current loop. Switch position 8 is not used. Refer to the switch summary table of figure 6 for the proper settings of SW5(SW6) which will meet your particular application needs.

#### 1.4.6 SW7-Port #1 and Port #2 Receive Current Select

SW7 is a six position switch which is used to configure the current loop receive circuitry. Positions 1, 2, 3 are used by serial port #1 and positions 4, 5, 6 are used by serial port #2. SW7 keeps the current constant through the receiving circuit by switching a shunt resistor in parallel with it. Refer to the switch summary table of figure 6 for the proper settings of SW7 which will meet your particular application needs.

#### 1.4.7 SW8(SW9)-Port #1(#2) Receive Select

Serial port #1(#2) uses the eight position dip switch, SW8(SW9), to select either active or passive reception (active reception provides the current in the loop whereas passive reception does not) and the value of current (20, 30, or 60 mA) when the active option is selected. Passive reception is controlled by switch positions 1&2 and active reception is controlled by switch positions 3&4. Switch positions 5-7 configure the value of current within the current loop. Switch position 8 is not used. Refer to the switch summary table of figure 8 for the proper settings of SW8(SW9) which will meet your particular application needs.

<b>J1</b>	
<b>Function</b>	<b>Connect</b>
Clock/1	2 & 5
Clock/2	2 & 3 and 4 & 5
Clock/5	1 & 2 and 4 & 5
Clock/10	1 & 2, 3 & 6 and 4 & 5

<b>J2 - J3</b>	
<b>Function</b>	<b>Connect</b>
IRQ2	1 & 7
IRQ3	2 & 8
IRQ4	3 & 9
IRQ5	4 & 10
IRQ6	5 & 11
IRQ7	6 & 12

<b>J4 - J5</b>	
<b>Function</b>	<b>Connect</b>
PC Power Supplu	2 & 5
Isolated Power Supply	1 & 2

Figure 4: Jumper Summary

<b>SW5 - SW6</b>	
<b>Function</b>	<b>Switches On</b>
Passive Transmit	1 & 2
20 mA Active Transmit	3 & 4 & 5
30 mA Active Transmit	3 & 4 & 5 & 6
60 mA Active Transmit	3 & 4 & 5 & 6 & 7

SW7 - Port #1	
Function	Switches On
20 mA Receive	1
30 mA Receive	2
60 mA Receive	3

SW7 - Port #2	
Function	Switches On
20 mA Receive	4
30 mA Receive	5
60 mA Receive	6

SW8 - SW9	
Function	Switches On
Passive Receive	1 & 2
20 mA Receive	3 & 4 & 5
30 mA Receive	3 & 4 & 5 & 6
60 mA Receive	3 & 4 & 5 & 6 & 7

Figure 5: Switch Summary Table

#### 1.4.7.1 Factory Jumper and Switch Configurations

JUMPERS			
J1	J2 (J3)	J4	J5
1 & 2	3 & 9	2 & 3	2 & 3
3 & 6	(2 & 8)		
4 & 5			

J1 - Divide by 10 selected for 18.432 MHz UART clock frequency

J2 - IRQ4 is selected as the interrupt for serial port #1

J3 - IRQ3 is selected as the interrupt for serial port #2

J4 & J5 - Computers power supply generates the loop current

SWITCHES		
SW5 (SW6)	SW7	SW8 (SW9)
3 & 4 & 5	1 & 4	1 & 2
3 & 4 & 5		(1 & 2)

SW5 - Active transmission with 20mA loop current for serial port #1

SW6 - Active transmission with 20mA loop current for serial port #2

SW7 - 20mA loop current for serial port #1 and serial port #2

SW8 - Passive reception for serial port #1

SW9 - Passive reception for serial port #2

## 1.5 External Connections

Connections to the outside world are made available via two DB-9 connectors. These connectors provide excellent shielding against environmental noise to aid in reliable communication. A pin-out of the DB-9 connector is illustrated in figure 9. A detailed description of each signal is provided for convenient reference.

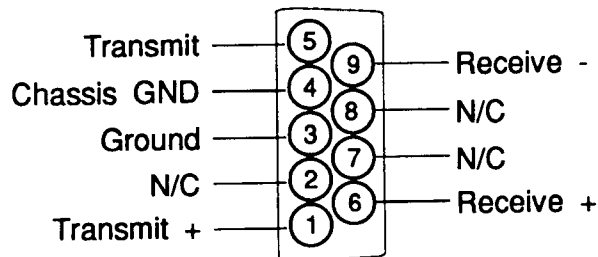


Figure 6: DB-9 Connector Pinouts

Pin #	Signal Name	Description
1	TRANSMIT+	TRANSMIT SERIAL DATA
2	NO CONNECTION	
3	GROUND	SIGNAL RETURN PATH
4	CHASSIS	GROUND CHASSIS GROUND
5	TRANSMIT-	TRANSMIT SERIAL DATA
6	RECEIVE +	RECEIVE SERIAL DATA
7		NO CONNECTION



8		NO CONNECTION
9	RECEIVE	RECEIVE SERIAL DATA

### 1.6 Current Loop Driver Schematics

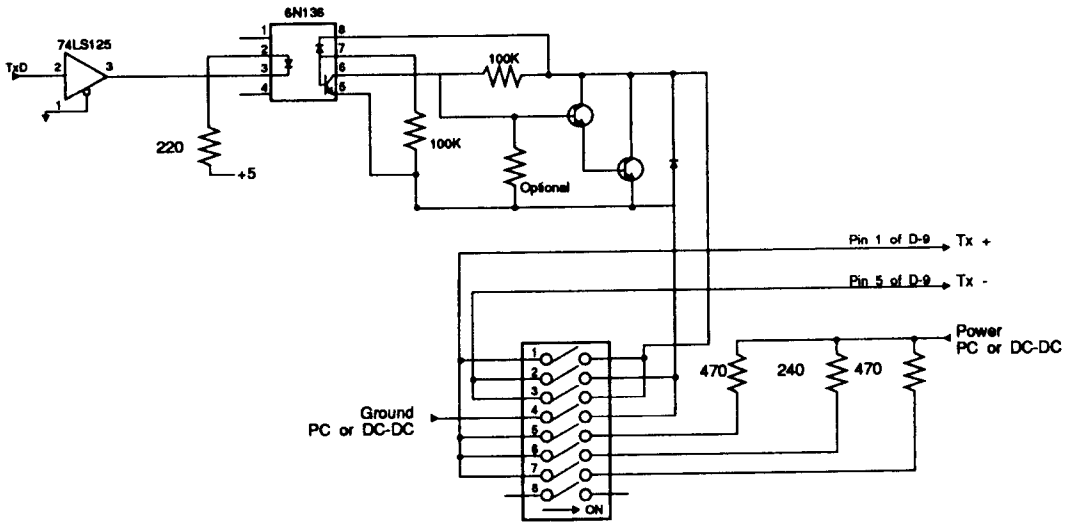


Figure 7: Transmission Circuit

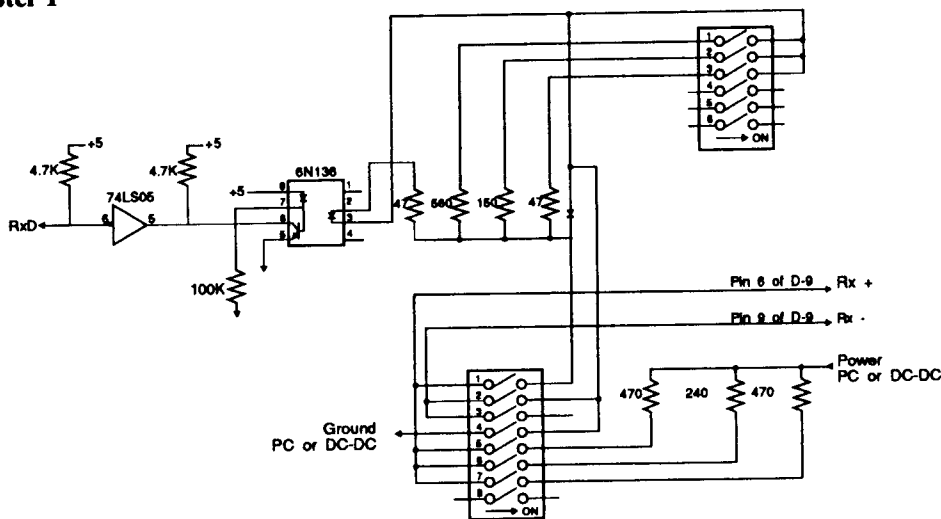


Figure 8: Receiving Circuit

## 1.7 Detailed Information on the 8250/16450 UARTS

The following pages are a brief summary of the internal registers available within the 8250 and the 16450 asynchronous UART's. The address map for the serial port registers has been reproduced again for convenient reference.

DLAB	A2	A1	A0	Register Description
0	0	0	0	Receive buffer (read only) Transmitter holding register (write only)
0	0	0	1	Interrupt enable
x	0	1	0	Interrupt identification (read only) FIFO control* (write only)
x	0	1	1	Line control
x	1	0	0	MODEM control
x	1	0	1	Line status
x	1	1	0	MODEM status
x	1	1	1	Scratch
1	0	0	0	Divisor latch (LSB)
1	0	0	1	Divisor latch (MSB)

### 1.7.1 Line Control Register

The bit definitions for this register are as follows:

**Bits 0 & 1:** Specifies word length in transmitted and received characters.

BIT1	BIT2	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- Bit 2:** Specifies the number of stop bits in a transmitted or received character. If bit 2 is 0, then 1 stop bit is generated regardless of word length. If bit 2 is 1 when the word length is 5 bits, 1.5 stop bits are generated. If bit 2 is 1 when the word length is 6, 7, or 8 bits, 2 stop bits are generated.
- Bit 3:** Parity Enable Bit. If set to 0, no parity bit is generated. If set to 1, a parity bit is generated.
- Bit 4:** Even/Odd Parity Select. If bit 3 is a 1 and bit 4 is a 0, odd parity is generated. If bit 3 is a 1 and bit 4 is a 1, even parity is generated.
- Bit 5:** Stick Parity Bit. If bit 3 is a 1 and bit 5 is a 1 then a parity transmitted and then received in an opposite state indicated by bit 4.
- Bit 6:** Set Break Control Bit. When set to a 1, SOUT (pin11) is set to a 0 state.
- Bit 7:** Divisor Latch Enable Bit (DLAB). Must be set to 1 to access the divisor latches. These latches set the baud rate depending on the value written to them. Must be set to 0 to access the receiver buffer, transmitting holding register or the interrupt enable register.

### 1.7.2 Line Status Register

The bit definitions for this register are as follows:

- Bit 0:** Data Ready Indicator. When set to 1, data is present in the receive buffer. Bit 0 is cleared upon reading the receive buffer by writing a 0 to it.
- Bit 1:** Overrun Error. When set to a 1, data was not read from the receive buffer fast enough and was written over by the next incoming data byte. This bit is reset to a 0 by reading the line status register.

- Bit 2:** Parity Error. When set to a 1, indicates that the received data does not have the correct parity as selected by bit 4 of the line control register. This bit is reset to a 0 by reading the line status register.
- Bit 3:** Framing Error. When set to a 1, indicates that the stop bit following the last data bit or parity bit was a 0. This bit is reset to a 0 by reading the line status register.
- Bit 4:** Break Interrupt Indicator. When set to a 1, indicates the receive data input to the receive buffer has been in a 0 state for longer then the full word transmission time. Reset to a 0 upon reading the line status register.
- Bit 5:** Transmitter Holding Register Empty: When set to a 1, indicates that the transmitter holding register has moved its present character to the transmitter shift register and is ready for a new character. Reset to a 0 when a new character is written to the transmitter holding register.
- Bit 6:** Transmitter Shift Register Empty. When set to a 1, indicates that the transmitter shift register is ready to receive a new character. Reset to a 0 when a transfer from the transmitter holding register to the transmitter shift register takes place.
- Bit 7:** Set to a 0.

### 1.7.3 Interrupt Identification Register

The bit definitions for this register as as follows:

- Bit 0:** When set to a 0, indicates that an interrupt is pending. When set to a 1, indicates that no interrupt is pending.
- Bits 1 & 2:** These two bits identify the interrupt which is pending when bit 0 is set to a 0.

<b>BIT2</b>	<b>BIT1</b>	<b>Priority</b>	<b>Interrupt Type</b>
1	1	Highest	Receiver Line Flag
1	0	Second	Received Data Available
0	1	Third	Transmitter Holding Register Empty
0	0	Fourth	MODEM Status

### 1.7.4 Interrupt Enable Register

The bit definitions for this register are as follows:

- Bit 0:** When set to 1, Receive Data Interrupt is enabled.

- Bit 1:** When set to 1, Transmitting Holding Register Empty Interrupt is enabled.
- Bit 2:** When set to 1, Line Status Interrupt is enabled.
- Bit 3:** When set to 1, Modem Status Interrupt is enabled.
- Bits 4-7:** Set to logic 0.

### 1.7.5 Modem Control Register

The bit definitions for this register are as follows:

- Bit 0:** Data Terminal Ready bit. When set to 1, pin 33 is forced to a logic 0. When set to 0, pin 33 is forced to a logic 1.
- Bit 1:** Request to Send bit. When set to 1, pin 32 is forced to a logic 0. When set to 0, pin 32 is forced to a logic 1.
- Bit 2:** Output 1 bit. When set to a 1, pin 34 is forced to a logic 0. When set to 0, pin 34 is forced to a logic 1.
- Bit 3:** Output 2 bit: When set to a 1, pin 31 is forced to a logic 0. When set to 0, pin 31 is forced to a logic 1.
- Bit 4:** Loopback bit: When set to a 1, the transmitter shift register is connected to the receiver shift register. Therefore all characters transmitted are immediately received to verify transmit and receive data paths.
- Bits 5-7:** Set to logic 0.

### 1.7.6 Modem Status Register

The bit definitions for this register are as follows:

- Bit 0:** Delta Clear to Send (DCTS) bit. When set to 1, indicates the Clear to Send input (pin 36) has changed since the last time it was read by the CPU. Reset to a 0 upon reading the Modem Status Register.
- Bit 1:** Delta Data Set Ready (DDSR) bit. When set to 1, indicates the Data Set Ready input (pin 37) has changed since the last time it was read by the CPU. Reset to a 0 upon reading the Modem Status Register.
- Bit 2:** Trailing Edge of Ring Indicator (TERI) bit. When set to 1, indicates that the state of the Ring Indicator input (pin 39) has changed from a logic 1 to a logic 0. Reset to a 0 upon reading the Modem Status Register.
- Bit 3:** Delta Received Line Signal Detector (DRLSD) bit. When set to 1, indicates that the Carrier Detect input (pin 38) has changed since the last time it was read by the CPU. Reset to a 0 upon reading the Modem Status Register.

- Bit 4:** Complement of the Clear to Send input (pin 36).  
**Bit 5:** Complement of the Data Set Ready input (pin 37).  
**Bit 6:** Complement of the Ring Indicator input (pin 39).  
**Bit 7:** Complement of the Carrier Detect input (pin 38).

### 1.7.7 Divisor Latch Values to Select Baud Rates

The following table lists divisor latch settings for common baud rates using an 1.8432 Mhz input clock.

Desired Baud Rate	Divisor Latch Value	Error Between Desired and Actual Value (%)
50	2304	—
75	1536	—
110	1047	0.026
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

## 1.8 Hardware Installation

1. Set addressing, interrupts and output configuration jumpers on the card.
2. Turn unit off.
3. Remove system cover as instructed in the computer reference guide.
4. Insert card into a vacant slot following the guidelines for installation.
5. Replace system cover.
6. Plug computer into wall outlet.

## 1.9 Software Installation

### 1.9.1 DOS Installation

This section briefly describes some of the files contained on the installation disk. Particularly:

- COMDRIVE.SYS
- QMODE.COM
- QCFG.EXE

The files on this disk are intended to be used with IOtech's multi-port ASYNC boards.

#### COMDRIVE.SYS

This program is installed with CONFIG.SYS and should be located at [C:\COMDRIVE.SYS]. COMDRIVE allows for the use of COM1 through COM34 as DOS devices. This means that 'COPY \*.\* COM5' (assuming that the board is there and it is configured) would work through DOS. COMDRIVE is written to be used with IOtech's multi-port async boards.

To install COMDRIVE.SYS add the following line to your CONFIG.SYS file:

```
device=C:\COMDRIVE.SYS
```

(or the actual location of the program COMDRIVE.SYS.)

#### QCFG.EXE

This program is used to maintain the COMDRIVE device driver.

The port addresses of COMDRIVE are configurable and need to be defined before any multi-port board will operate properly with QMODE.COM and DOS. After the multi port

board is installed into the PC, COMDRIVE.SYS needs to be configured to recognize it. To do this the base address of the installed multi-port board(s) needs to be known.

Let's assume that the multi-port board has a base address of 300H (default), and let's also assume that it is a COM232/4PC QUAD PORT board. This would put port 1 of the board at a base address of 300H, port 2=308H, port 3=310H, and port 4=318H. Lastly, assume standard COM1 and COM2 boards are already installed in the PC.

To get COM3 up and running enter 'COM3=300' from the command line of QCFG. This will pipe data that goes from DOS COM3 to IOtech's multi-port board port 1. Then, to get COM4 activated, the command 'COM4=308' needs to be issued from QCFG, and so on for all other ports that are available.

## QMODE.COM

This utility is used to configure COM1-COM34. It operates like the DOS MODE command. To use QMODE the syntax is:

```
QMODE COMn[:]baud[, [parity][, [length][, [stopbits]
```

where:

*n* of COMn is 1 - 34 for the proper async logical port

*baud*: 110,150,300,600,1200,2400,4800,or 9600 (only first 2 characters required, ie. "96")

*parity*: E(ven) (default), N(one), O(dd)

*length*: 7 (default), 8

*stopbits*: 1 (default), 2

*Example*: QMODE COM18:2400,n,8,1

This command will configure logical COM address 18 to be 2400 baud, no parity, 8 bit, 1 stop bit.

### 1.9.1.1 Installing the Files

1. Add COMDRIVE to the CONFIG.SYS file  
DEVICE=COMDRIVE.SYS
2. Reboot, to recognize COMDRIVE.SYS
3. Run QCFG.EXE configure COMDRIVE.  
COM3=300  
:
4. Make sure, while in QCFG.EXE, to SAVE your modified configuration  
SAVE



Y (answer yes to both questions)

Y

:

5. Add QMODE commands to your AUTOEXEC.BAT for power-up configuration of the new COM PORTS  
QMODE COM3:96,e,7,1
6. Reboot.
7. Now all defined COM ports should be addressable.  
'COPY \*.\* COM3' will work properly

### 1.9.2 Windows Installation

To install the IOtech Windows 3.1 versions of the communications drivers, follow these steps:

1. Select Run from either File Manager or Program Manager. This is in the File Menu for either of these.
2. Type a:\setup. This works if your source diskette is inserted in drive A. Use the appropriate drive letter of the disk drive for your source diskette.
3. Setup will install the new device drivers and will modify the appropriate Windows system files. There is an additional application, Com Config, which is placed in the IOtech App group file.
4. Run the IOtech Com Config application. This will allow you to configure the device drivers for things such as the I/O address, IRQ, baud rate, handshaking, etc. This application incorporates context sensitive help.